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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,176	03/02/2004	Kenichi Iizuka	107337-00106	3546

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EXAMINER	
VIDWAN, JASJIT S	
ART UNIT	PAPER NUMBER
2182	

NOTIFICATION DATE	DELIVERY MODE
08/06/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

DCIPDocket@arentfox.com
IPMatters@arentfox.com
Patent_Mail@arentfox.com

Office Action Summary	Application No.	Applicant(s)	
	10/790,176	IIZUKA ET AL.	
	Examiner	Art Unit	
	JASJIT S. VIDWAN	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *11-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *02/03/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 04/29/09 have been fully considered but they are not persuasive. Applicant argues that as amended, prior art of record fails to teach the system including a status indicator for the buffer and the register indicating when the buffer is full of data and that new information has been written to the register.

2. With respect to above arguments, **Examiner disagrees**. As amended, Applicant includes the limitation of having status register indicating information regarding the status of the buffer and the register when the buffer is full and new information has been added to the register. Gulick teaches having a status register generating an interrupt when new byte information is added to the data buffers (and the register as it would follow). The bus bridge provides the status data from the register to the status buffer within the bus bridge's transmit port. The bus device interface sets a data available bit or generates an interrupt to a device DSP or functional unit when the data are received at the designated receive port **[see Gulick, Col. 16, Lines 8-20]**.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 3, 4, 5, 6, 7, 8, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Preiss et al, U.S. Patent No: 6,757,763 **[herein after Preiss]** and further in view of Gulick, U.S. Patent No: 5,898,848 [hereinafter Gulick]

3. **As per claims 1, 6 and 7**, Preiss teaches an information-processing unit **[Fig. 1, element 100]** for carrying out information processing in cooperation with an external host **[Fig. 1, element 103]** apparatus connected thereto via an external connection bus **[Fig. 1, element 107]**, comprising:

a. Internal CPU **[Fig. 1, element 102, "UDC"]**

b. Receive buffer for storing only receive data received from said external host apparatus **[Fig. 2b & 8, element 800, "8-Byte Receive FIFO"]**

Preiss teaches the above limitations, however fails to explicitly disclose storing the communication control information in a register and further transferring the communication data (stored in the Data buffer) in addition to communication control information (stored in the transfer registers) to the destination device. Gulick of analogous art teaches storing transfer information in the transfer register **[see Gulick, Fig. 17, element 5076]** and further only communication data in a buffer **[see Gulick Fig. 17, element 5074]**. On the same token, it would have been obvious to include data end information with the target address in order to indicate end of the address. Control circuit **[Fig. 1, 105, "EPEC" – Gulick – Fig. 17, element 5072]** for passing the receive data stored in said receive register to said internal CPU and passing the receive communication control information stored in said receive register to said internal CPU **[Col. 3, Line 50 – Col. 4, Line 16, 'IN Transaction (Device to host)]**, and further passing the transmit data stored in said transmit buffer to said external host apparatus and passing transmit communication control information stored in said transmit register to said external host apparatus **[Col. 4, Lines 17-54, "Out Transaction (Host to Device)]**, wherein the second device performs an appropriate receive process according to the control information **[see Col. 3, Lines 9-18 *– Above limitation is also taught by Gulick – Summary – Col. 4, Lines 1-20*]**. In addition, Gulick teaches including a status register storing information indicating a status of the buffer and the register, the status indicating that the buffer is full of data and that new information has been written in the register **[see Gulick, Col. 16, Lines 8-20]**.

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the two teachings in order to provide a more efficient bus bridge interconnect architecture for multimedia-related devices for interconnection and for interfacing to a standard

bus **[see Gulick, Col. 2, Lines 1-9]**. It is for this reason that one of ordinary skill in the art at the time of Applicant's invention would have been motivated to combine the two teachings.

4. **As per claim 2**, Preiss teaches an inter-bus communication interface device wherein said buffer is of a type that outputs data in the order that the data are stored **[Col. 1, Lines 35-40, "FIFO –First in First Out"]**.

5. **As per claim 3**, Preiss as modified by Gulick teaches an inter-bus communication interface device wherein said buffer includes a plurality of buffer areas, said buffer areas being alternately [As data moves across buffer areas, the location the data is stored will be alternately changed through the buffer] used in storing the communication data **[Col. 2, Lines 50-56]**.

6. **As per claim 4**, Preiss as modified by Gulick teaches communication interface device wherein said control circuit outputs an interrupt signal to the second device immediately after the communication control information is stored in said register **[see Gulick Col. 4, Lines 10-15]**.

7. **As per claim 5 and 9**, Preiss teaches communication interface device further including a status register for storing information indicative of whether or not un-transmitted data exists in said register **[Col. 5 Lines 26-35]** and wherein said control circuit updates the information in said status register, when new data is stored in said register, or when data in said buffer is read out by the second device **[Col. 5, Lines 41-45]**.

8. **As per claim 8**, Preiss teaches information processing unit wherein said control circuit outputs an interrupt signal to said internal CPU, when said receive buffer is full of the receive data, or when the receive communication control information is stored in said receive register **[Col. 5, Lines 26-35]**.

9. **As per claim 10**, Preiss teaches information processing unit wherein said control circuit outputs a transmit data-related request signal for requesting reception of the transmit data, to said external host apparatus, when data is stored in said transmit buffer or said transmit register **[Col. 3, Lines 51-59]**.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASJIT S. VIDWAN whose telephone number is (571)272-7936. The examiner can normally be reached on 8am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tariq Hafiz can be reached on 571.272.6729. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. S. V./
Examiner, Art Unit 2182

/Tariq Hafiz/
Supervisory Patent Examiner, Art Unit 2182